

# ALIGNMENT MARK AND EXPOSURE ALIGNMENT SYSTEM AND METHOD USING THE SAME

## Related Applications

This application is a divisional of copending U.S. application serial number 09/906,306, filed on July 16, 2001, <sup>PAT 6,667,253</sup> the contents of which are incorporated herein in their entirety by reference.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to an alignment mark and an alignment mark design method by which wafers are aligned to correspond with masks in an exposure aligning system.

### 2. Description of the Related Art

Generally, semiconductor devices are fabricated by performing repeated and selective processes such as patterning, etching, diffusing, metal-deposition, etc., to form one or more circuit patterning layers on a wafer. The deposition of circuit patterning layers requires that previously formed circuit patterning layers be aligned accurately.

In the alignment relationship of wafers, the alignment marks formed on exposure field regions EF<sub>n</sub> or scribe lines SCL of a wafer are illuminated by a light source and reflect diffracted light rays. The diffracted light rays from the alignment marks are detected to generate a photoelectric signal which is used to detect the position of the wafer. The position state of the wafers is checked and the wafers are aligned by an alignment means to